CLAIMS

We claim:

1. An electrical circuit comprising:

an amplifying transistor comprising a base terminal coupled to an input node; and

a power control circuit, wherein the power control circuit comprises:

a sense transistor comprising a base terminal and a collector terminal, wherein the base terminal is coupled to the base terminal of the amplifying transistor, the collector terminal is coupled to a ground via a capacitor, and the collector terminal is coupled to a reference voltage source via a first resistor;

a first error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first error amplifier is coupled to the collector of the sense transistor, and the output terminal of the first error amplifier is coupled to the input node;

a second error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second error amplifier is coupled to the output terminal of the second error amplifier via a second resistor, the first input terminal of the second error amplifier is coupled to a control voltage source via a third resistor, and the output terminal of the second error amplifier is coupled to the second input terminal of the first error amplifier; and

a fourth resistor and a fifth resistor coupled in series between the reference voltage source and the ground, wherein the second input terminal of the second error amplifier is coupled to a node between the fourth and the fifth resistors, and wherein the ratio of the resistance of the fourth resistor to the resistance of the fifth resistor is about equal to the ratio of the resistance of the second resistor to the resistance of the third resistor.

2. The circuit of claim 1, wherein the base terminal of the amplifying transistor is coupled to the input node via a ballast circuit.

3. The circuit of claim 1, wherein the output of the error amplifier is coupled to the input node via an inductor.

4. The circuit of claim 1, wherein the output of the error amplifier is coupled to the input node via a sixth resistor.

5. The circuit of claim 1, wherein the input node is connected to receive a radio frequency input signal.

6. The circuit of claim 1, wherein the collector of the sense transistor is directly connected to one electrode of the capacitor, and a second electrode of the capacitor is directly connected to the ground.

7. The circuit of claim 1, wherein the power control voltage source comprises a digital-to-analog converter.

8. An electrical circuit comprising:

an amplifying transistor comprising a base terminal coupled to an input node; and

a power control circuit, wherein the power control circuit comprises:

a sense transistor comprising a base terminal and a collector terminal, wherein the base terminal is coupled to the base terminal of the amplifying transistor, the collector terminal is coupled to a ground via a capacitor, and the collector terminal is coupled to a reference voltage source via a first resistor;

an error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal is coupled to the collector of the sense transistor, the first input terminal is coupled to a control voltage source via a second resistor, and the output terminal of the first error amplifier is coupled to the input node; and

a third resistor and a fourth resistor coupled in series between the reference voltage source and the ground, wherein the second input of the error amplifier is coupled to a node between the third and the fourth resistors, and wherein the ratio of the resistance of the first resistor to a resistance of the second resistor is about equal to the ratio of the resistance of the third resistor to a resistance of the fourth resistor.

9. The circuit of claim 8, wherein the base terminal of the amplifying transistor is coupled to the input node via a ballast circuit.

10. The circuit of claim 8, wherein the output of the error amplifier is coupled to the input node via an inductor.

11. The circuit of claim 8, wherein the output of the error amplifier is coupled to the input node via a sixth resistor.

12. The circuit of claim 8, wherein the input node is connected to receive a radio frequency input signal.

13. The circuit of claim 8, wherein the collector of the sense transistor is directly connected to one electrode of the capacitor, and a second electrode of the capacitor is directly connected to the ground.

14. The circuit of claim 8, wherein the power control voltage source comprises a digital-to-analog converter.

15. An electrical circuit comprising:

an amplifying transistor comprising a base terminal coupled to an input node; and

a power control circuit, wherein the power control circuit comprises:

a sense transistor comprising a base terminal and a collector terminal, wherein the base terminal is coupled to the base terminal of the amplifying transistor, the collector terminal is coupled to a ground via a capacitor, and the collector terminal is coupled to a reference voltage source via a first resistor;

a first error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first error amplifier is coupled to the collector of the sense transistor, and the output terminal of the first error amplifier is coupled to the input node;

a current source transistor comprising a base terminal, an emitter terminal, and a collector terminal, wherein the emitter terminal of the current source transistor is coupled to the ground via a second resistor, the collector terminal of the current source resistor is coupled to the reference voltage source via a third resistor, and the collector terminal of the current source transistor is coupled to the second input terminal of the first error amplifier;

a second error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the output terminal of the second error amplifier is coupled to the base of the current source transistor, the first input terminal of the second error amplifier is coupled to the emitter of the current source transistor, and the second input terminal of the second error amplifier is coupled to a control voltage source.

16. The circuit of claim 15 comprising a fourth resistor and a fifth resistor coupled in series between the control voltage source and the ground, wherein the second input terminal of the second error amplifier is coupled to a node between the fourth and the fifth resistors.

17. The circuit of claim 15, wherein the base terminal of the amplifying transistor is coupled to the input node via a ballast circuit.

18. The circuit of claim 15, wherein the output of the error amplifier is coupled to the input node via an inductor.

19. The circuit of claim 15, wherein the output of the error amplifier is coupled to the input node via a sixth resistor.

20. The circuit of claim 15, wherein the input node is connected to receive a radio frequency input signal.

21. The circuit of claim 15, wherein the collector of the sense transistor is directly connected to one electrode of the capacitor, and a second electrode of the capacitor is directly connected to the ground.

22. The circuit of claim 15, wherein the power control voltage source comprises a digital-to-analog converter.

23. A method for sensing and controlling the power of a signal output by an amplifying transistor, comprising the acts of:

coupling a base terminal of a sense transistor to a base terminal of the amplifying transistor;

creating a sense current in the sense transistor, wherein the sense current corresponds to an output current of the amplifying transistor, and wherein the sense current is sourced by a reference voltage source and a control voltage source;

creating a divided voltage of a voltage output by the reference voltage source; and

outputting a control signal to a base terminal of the amplifying transistor, wherein the control signal is associated with a difference between the divided voltage and a sense voltage, the sense voltage being associated with a DC portion of the sense current and with a power control voltage, and wherein the control signal controls the output current of the amplifying transistor.

24. The method of claim 23, wherein the signal output by the amplifying transistor is a cellular telephone radio frequency signal.

25. The method of claim 23 further comprising the act of changing the power of the signal output by the amplifying transistor by changing the power control voltage.

26. The method of claim 23 further comprising the act of using a digital to analog converter to create the power control voltage.

27. An electrical circuit comprising:

a plurality of amplifying transistors, wherein each unique amplifying transistor comprises a base terminal and a collector terminal, and wherein the collector terminals of each unique amplifying transistor are coupled together; and

a power control circuit, wherein the power control circuit comprises:

a plurality of sense transistors, wherein each unique sense transistor comprises a base terminal and a collector terminal, wherein the base terminal of each unique sense transistor is coupled to the base terminal of a unique corresponding amplifying transistor, and wherein the collector terminals of the sense transistors are coupled together; and

an error amplifier circuit, wherein the error amplifier circuit is coupled to receive a sense voltage from the collector terminals of the sense transistors, and is coupled to output a bias control signal to the base terminals of the amplifying transistors.

28. The circuit of claim 27, wherein the error amplifier circuit comprises an error amplifier, wherein the error amplifier comprises a first input terminal coupled to the collectors of the sense transistors, a second input terminal coupled to a power control voltage source, and an output terminal coupled to output the bias control signal.

29. The circuit of claim 27, wherein the error amplifier circuit comprises:

a first error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first error amplifier is coupled to the collectors of the sense transistors, and the output terminal of the first error amplifier is coupled to the base terminals of the amplifying transistors;

a second error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second error amplifier is coupled to the output terminal of the second error amplifier via a first resistor, the first input terminal of the second error amplifier is coupled to a control voltage source via a second resistor, and the output terminal of the second error amplifier is coupled to the second input terminal of the first error amplifier; and

a third resistor and a fourth resistor coupled in series between the reference voltage source and the ground, wherein the second input terminal of the second error amplifier is coupled to a node between the third and the fourth resistors, and wherein the ratio of the resistance of the third resistor to the resistance of the

fourth resistor is about equal to the ratio of the resistance of the first resistor to the resistance of the second resistor.

30. The circuit of claim 27, wherein the collectors of the sense transistors are coupled to a reference voltage source via a first resistor, and wherein the error amplifier circuit comprises:

an error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal is coupled to the collectors of the sense transistors, the first input terminal is coupled to a control voltage source via a second resistor, and the output terminal of the error amplifier is coupled to the base terminals of the amplifying transistors; and

a third resistor and a fourth resistor coupled in series between the reference voltage source and a ground, wherein the second input of the error amplifier is coupled to a node between the third and the fourth resistors, and wherein the ratio of the resistance of the first resistor to a resistance of the second resistor is about equal to the ratio of the resistance of the third resistor to a resistance of the fourth resistor.

31. The circuit of claim 27, wherein the error amplifier circuit comprises:

a first error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first error amplifier is coupled to the collectors of the sense transistors, and the output terminal of the first error amplifier is coupled to the base terminals of the amplifying transistors;

a current source transistor comprising a base terminal, an emitter terminal, and a collector terminal, wherein the emitter terminal of the current source transistor is coupled to a ground via a first resistor, the collector terminal of the current source transistor is coupled to the reference voltage source via a second resistor, and the collector terminal of the current source transistor is coupled to the second input terminal of the first error amplifier; and

a second error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the output terminal of the second error amplifier is coupled to the base of the current source transistor, the first input terminal of the second error amplifier is coupled to the emitter of the current source

transistor, and the second input terminal of the second error amplifier is coupled to a control voltage source.

32. The circuit of claim 27, wherein a sense transistor is paired with every second or every fourth amplifying transistor.

33. The circuit of claim 27, wherein the base terminal of each unique amplifying transistor is coupled to the base terminal of a corresponding unique sense transistor.

34. The circuit of claim 33, wherein the error amplifier circuit comprises an error amplifier, wherein the error amplifier comprises a first input terminal coupled to the collectors of the sense transistors, a second input terminal coupled to a power control voltage source, and an output terminal coupled to output the bias control signal.

35. The circuit of claim 33, wherein the error amplifier circuit comprises:

a first error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first error amplifier is coupled to the collectors of the sense transistors, and the output terminal of the first error amplifier is coupled to the base terminals of the amplifying transistors;

a second error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second error amplifier is coupled to the output terminal of the second error amplifier via a first resistor, the first input terminal of the second error amplifier is coupled to a control voltage source via a second resistor, and the output terminal of the second error amplifier is coupled to the second input terminal of the first error amplifier; and

a third resistor and a fourth resistor coupled in series between the reference voltage source and the ground, wherein the second input terminal of the second error amplifier is coupled to a node between the third and the fourth resistors, and wherein the ratio of the resistance of the third resistor to the resistance of the fourth resistor is about equal to the ratio of the resistance of the first resistor to the resistance of the second resistor.

36. The circuit of claim 33, wherein the collectors of the sense transistors are coupled to a reference voltage source via a first resistor, and wherein the error amplifier circuit comprises:

an error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal is coupled to the collectors of the sense transistors, the first input terminal is coupled to a control voltage source via a second resistor, and the output terminal of the error amplifier is coupled to the base terminals of the amplifying transistors; and

a third resistor and a fourth resistor coupled in series between the reference voltage source and a ground, wherein the second input of the error amplifier is coupled to a node between the third and the fourth resistors, and wherein the ratio of the resistance of the first resistor to a resistance of the second resistor is about equal to the ratio of the resistance of the third resistor to a resistance of the fourth resistor.

37. The circuit of claim 33, wherein the error amplifier circuit comprises:

a first error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first error amplifier is coupled to the collectors of the sense transistors, and the output terminal of the first error amplifier is coupled to the base terminals of the amplifying transistors;

a current source transistor comprising a base terminal, an emitter terminal, and a collector terminal, wherein the emitter terminal of the current source transistor is coupled to a ground via a first resistor, the collector terminal of the current source transistor is coupled to the reference voltage source via a second resistor, and the collector terminal of the current source transistor is coupled to the second input terminal of the first error amplifier; and

a second error amplifier comprising a first input terminal, a second input terminal, and an output terminal, wherein the output terminal of the second error amplifier is coupled to the base of the current source transistor, the first input terminal of the second error amplifier is coupled to the emitter of the current source transistor, and the second input terminal of the second error amplifier is coupled to a control voltage source.

38. A method for sensing and controlling the power of a signal output by a plurality of amplifying transistors, wherein each unique amplifying transistor comprises a base terminal and a collector terminal, and wherein the collector terminals of the amplifying transistors are coupled together, the method comprising the acts of:

providing a plurality of sense transistors, wherein each unique sense transistor comprises a base terminal and a collector terminal;

forming a plurality of sense and amplifying transistor pairs by coupling the base terminal of each unique sense transistor to the base terminal of an amplifying transistor;

coupling the collector terminals of the sense transistors together;

outputting a sense voltage from the coupled sense transistor collectors to an error amplifier circuit; and

outputting a control signal from the error amplifier circuit to the base terminals of the amplifying transistors, wherein the control signal is associated with a difference between a power control voltage and the sense voltage, and wherein the control signal controls the output current of the amplifying transistors.

39. The method of claim 38, wherein the number of sense and amplifying transistors is the same.

40. The method of claim 38, wherein a sense transistor is coupled to every second or every fourth amplifying transistor.

41. The method of claim 38, wherein a sense transistor is coupled to only selected amplifying transistors likely to operate at higher temperatures than remaining amplifying transistors.

42. The method of claim 38 further comprising the act of making the control signal independent of variations in a reference voltage received by the sense transistors.

43. The method of claim 38 further comprising the act of changing the power of the signal output by the amplifying transistors by changing the power control voltage.

44. The method of claim 38 further comprising the act of using an analog to digital converter to set the power control voltage.

45. The method of claim 38, wherein the signal output by the amplifying transistors is a cellular telephone radio frequency signal.